## IN THE CLAIMS

Please amend the claims as follows.

1. (Original) A circuit comprising:

a booth encoder circuit having a plurality of transistors to receive a plurality of multiplier bits and complements of said plurality of multiplier bits, and a plurality of logic circuits coupled to ones of said plurality of transistors to output Booth encoded signals; and

a partial products generating circuit having a first multiplexing device to receive said Booth encoded signals and to provide a first partial products output, and a second multiplexing device to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output.

2. (Original) The circuit of claim 1, wherein said plurality of logic circuits includes a recoding circuit.

3. (Original) The circuit of claim 1, wherein said first multiplexing device further to receive a signal corresponding to a first bit of a multiplicand and a signal corresponding to a complement of said first bit.

4. (Original) The circuit of claim 3, wherein said second multiplexing device further to receive a signal corresponding to a second bit of said multiplicand and a signal corresponding to a complement of said second bit.

5. (Currently Amended) A Booth encoder circuit comprising:

a plurality of transistors to receive a plurality of multiplier bits and complements of said plurality of multiplier bits; and

a plurality of logic circuits coupled to ones of said plurality of transistors to output Booth encoded signals, wherein said Booth encoded signals are substantially gate delay-matched ~~at an~~ from the transistors to the output of said Booth encoder circuit.

6. (Original) The Booth encoder circuit of claim 5, wherein said plurality of transistors comprise a first subcircuit, a second subcircuit, a third subcircuit, and a fourth subcircuit, and said plurality of logic circuits comprise first logic circuits, second logic circuits, third logic circuit and fourth logic circuits, said first subcircuit to receive two of said multiplier bits and complements of two multiplier bits, said first subcircuit to provide a signal to said first logic circuits, said first logic circuits to output two Booth encoded signals.

7. (Original) The Booth encoder circuit of claim 6, wherein said second subcircuit to receive one of said multiplier bits and complements of two multiplier bits, said second subcircuit to provide a signal to said second logic circuits, said second logic circuits to output one Booth encoded signal.

8. (Original) The Booth encoder circuit of claim 7, wherein said third subcircuit to receive two of said multiplier bits and complements of one multiplier bit, said third subcircuit to provide a signal to said third logic circuits, said third logic circuits to output one Booth encoded signal.

9. (Original) The Booth encoder circuit of claim 8, wherein said fourth subcircuit to receive two of said multiplier bits and complements of two multiplier bits, and to provide a signal to said fourth logic circuits based on said two of said multiplier bits and said complements of two multiplier bits, said fifth subcircuit to receive two of said multiplier bits and complements of two multiplier bits and to provide a signal to said fourth logic circuit based on said two of said multiplier bits and said complements of two multiplier bits, said fourth logic circuit to output one Booth encoded signal.

10. (Original) The Booth encoder circuit of claim 5, wherein said Booth encoded signals represent:

a multiply by zero;
a multiply by one;
a multiply by negative one;

a multiply by two; and

a multiply by negative two.

11. (Canceled)

12. (Original) The Booth encoder circuit of claim 5, wherein said circuit has a maximum of a three-gate delay from an input of said Booth encoder circuit to an output of said Booth encoder circuit.

13. (Currently Amended) A multiplier circuit comprising logic to receive a plurality of multiplier bits and complements of said multiplier bits, said logic to output Booth encoded signals based on said multiplier bits and complements of said multiplier bits, said logic configured to have a ~~maximum~~ <u>substantially matched delay</u> of three gate delays from an input of said multiplier circuit to an output of said multiplier circuit.

14. (Original) The multiplier circuit of claim 13, wherein said logic comprises a plurality of transistors, a plurality of NAND gates and a plurality of inverters.

15. (Original) The multiplier circuit of claim 14, wherein said NAND gates comprises two-input NAND circuits.

16. (Original) The multiplier circuit of claim 14, wherein at least said plurality of transistors form a first subcircuit, a second subcircuit, a third subcircuit, and a fourth subcircuit, and said NAND gates and said inverters form first logic circuits, second logic circuits, third logic circuit and fourth logic circuits, said first subcircuit to receive two of said multiplier bits and complements of two multiplier bits, said first subcircuit to provide a signal to said first logic circuits, said first logic circuits to output two Booth encoded signals.

17. (Original) The multiplier circuit of claim 16, wherein said second subcircuit to receive one of said multiplier bits and complements of two multiplier bits, said second subcircuit to provide a

signal to said second logic circuits, said second logic circuits to output one Booth encoded signal.

18. (Original) The multiplier circuit of claim 17, wherein said third subcircuit to receive two of said multiplier bits and complements of one multiplier bit, said third subcircuit to provide a signal to said third logic circuits, said third logic circuits to output one Booth encoded signal.

19. (Original) The multiplier circuit of claim 18, wherein said fourth subcircuit to receive two of said multiplier bits and complements of two multiplier bits and to provide a signal to said fourth logic circuits based on said two of said multiplier bits and said complements of two multiplier bits, said fifth subcircuit to receive two of said multiplier bits and complements of two multiplier bits and to provide a signal to said fourth logic circuit based on said two of said multiplier bits and said complements of two multiplier bits, said fourth logic circuit to output one Booth encoded signal.

20. (Original) The multiplier circuit of claim 13, wherein said Booth encoded signals represent:

a multiply by zero;
a multiply by one;
a multiply by negative one;
a multiply by two; and
a multiply by negative two.

21. (Original) The multiplier circuit of claim 13, wherein said Booth encoded signals are substantially delay-matched at an output of said multiplier circuit.

22. (Original) A circuit comprising logic to receive a plurality of multiplier bits and complements of said multiplier bits, said logic including a plurality of transistors, a plurality of NAND gates and a plurality of inverters configured to output delay-matched Booth encoded signals based on said multiplier bits and said complements.

23. (Original) The circuit of claim 22, wherein said logic is configured to have a maximum of three gate delays from an input of said circuit to an output of said circuit.

24. (Original) The circuit of claim 22, wherein said NAND gates comprise two-input NAND gates.

25. (Previously Presented) A Booth encoder circuit comprising:

a first subcircuit to receive at least one multiplier bit and complements of at least one multiplier bit, said first subcircuit to provide a signal to first logic circuits, said first logic circuits to output two Booth encoded signals;

a second subcircuit to receive at least one multiplier bit and complements of at least one multiplier bit, said second subcircuit to provide a signal to second logic circuits, said second logic circuits to output one Booth encoded signal;

a third subcircuit to receive at least one multiplier bit and complements of at least one multiplier bit, said third subcircuit to provide a signal to third logic circuits, said third logic circuits to output one Booth encoded signal;

a fourth subcircuit to receive at least one multiplier bit and complements of at least one multiplier bit, said fourth subcircuit to provide a signal to fourth logic circuits; and

a fifth subcircuit to receive at least one multiplier bit and complements of at least one multiplier bit, said fifth subcircuit to provide a signal to said fourth logic circuit, said fourth logic circuit to output one Booth encoded signal, and wherein said Booth encoded signals are substantially delay-matched at an output of said Booth encoder circuit.

26. (Original) The Booth encoder circuit of claim 25, wherein said circuit is configured to have a maximum of three gate delays from an input of said Booth encoder circuit to an output of said Booth encoder circuit.

27. (Original) The Booth encoder circuit of claim 25, wherein said first subcircuit, said second subcircuit, said third subcircuit, said fourth subcircuit and said fifth subcircuit each include a NAND gate and an inverter.

28. (Original) The Booth encoder circuit of claim 27, wherein said NAND gates comprises two-input NAND gates.

29. (Canceled)

30. (Original) A partial products generator circuit comprising:

a first multiplexing device having a plurality of first transistors to receive Booth encoded signals and to provide a first partial products output; and

a second multiplexing device having a plurality of second transistors to receive said Booth encoded signals and multiplexed data from said first multiplexing device and to provide a second partial products output.

31. (Original) The partial products generator circuit of claim 30, further comprising:

a third multiplexing device having a plurality of third transistors to receive said Booth encoded signals and multiplexed data from said second multiplexing device and to provide a third partial products output.

32. (Previously Presented) The partial products generator circuit of claim 30, wherein said plurality of first transistors comprise n-channel field-effect transistors (NFETs).

33. (Original) The partial products generator circuit of claim 30, wherein said first multiplexing device further to receive a signal corresponding to a first bit of a multiplicand and a signal corresponding to a complement of said first bit.

34. (Original) The partial products generator circuit of claim 33, wherein said second multiplexing device further to receive a signal corresponding to a second bit of said multiplicand and a signal corresponding to a complement of said second bit.

35. (Original) The partial products generator circuit of claim 30, wherein said plurality of first transistors comprise five transistors.

36. (Original) The partial products generator circuit of claim 30, wherein said multiplexed data comprises data from a previous bit of a multiplicand.

37. (Previously Presented) A partial products generator circuit comprising a multiplexing device to receive Booth encoded signals and to provide a first partial product output for a first bit of a multiplicand based at least on multiplexed data received from a previous multiplexing device.

38. (Original) The partial products generator circuit of claim 37, wherein said previous multiplexing device receives said Booth encoded signals and provides a second partial products output for a second bit of said multiplicand based at least on multiplexed data from another multiplexing device.

39. (Original) The partial products generator circuit of claim 38, wherein said multiplexing device further to receive a signal corresponding to said first bit of said multiplicand and a signal corresponding to a complement of said first bit.

40. (Original) The partial products generator circuit of claim 39, wherein said previous multiplexing device further to receive a signal corresponding to said second bit of said multiplicand and a signal corresponding to a complement of said second bit.